

ADCstamp – Compact AD Converter Module for Seamless FPGA Integration

Engineered for precision. Designed for speed. Built for integration.

The *ADCstamp* is the ideal building block (AD System-on-Module) for developers who need to integrate high-speed precision measurement channels—such as for power analysis of electric motors—into existing or new FPGA/CPU designs, without having to deal with the complexities of analog and digital signal path design.

The **5 kV galvanic isolation** ensures safe operation in all high-voltage applications. Clear design guidelines, FPGA source code examples, and fully equipped starter kits enable commissioning within minutes.

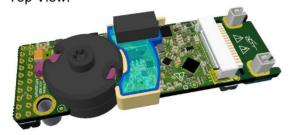


In short: ADCstamp delivers outstanding precision, rapid response times, and reliable measurements — a revolutionary solution for science and engineering.

- 24 Bit ADC with 4 MS/s sampling rate
- Integrated **preamplifiers** for up to **±1.5 kV** input range
- Industry-leading low noise and minimal distortion
- 5 kV reinforced galvanic isolation (1000V CAT II)
- Integrated sensor excitation: 0 to 5 mA (DAC adjustable)
- Complete FPGA starter kits available

ADCstamp® LTT1675A V3.0 2025:

Top View:



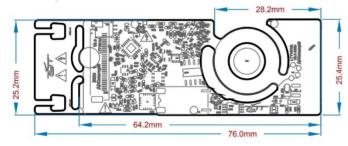
Bottom View:



Technical Specifications

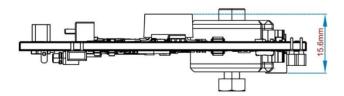
Analog Input	Characteristics	
Quantization	24 Bit	
Max. sample rate per channel	4 MSample/s/ch	
Max. Bandwidth per channel	DC – 1.7 MHz	
Filter	Analog: 1.7 MHz low pass filter. Digital: selectable	
Volt Input Ranges	± 250 mV ± 1500 V depending on external resistor	
Volt Input Impedance	external resistor: 10kΩ 10MΩ	
Volt Input Couplings	- Single-Ended with 3 gains (selectable by software) - Differential-Ended with 1 fixed gain	
Galvanic Isolation	± 5000 V	
Dynamic range Bandwidth	5 kHz = 114 dB 50 kHz = 114 dB 1 MHz = 96 dB	
ENOB (THD + noise) effektive Bits dB @ 125 kHz Sample Rate	typ 14.8 Bit -90 dB	
IEPE (ICP®) (optional)	Constant Current Supply: 0 5mA Input Coupling: external AC or DC	
Power Supply	Vsup = 12 VDC ± 5%, 2 W typical Vdd = 2.5 VDC 5.5 VDC, 0.3 W typical	
Environmental Temperature	+1 °C to +50 °C	
Sample Clock Input	16 MHz 32 MHz	
DCDC Clock Input	1 MHz 2 MHz (= 1/8 of Sample Clock)	
Dimensions	25.4 (w) x 76.0 (l) x 15.6 (h) mm	
Specifications are subject to change without notice	V3.0	

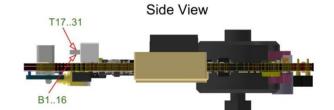




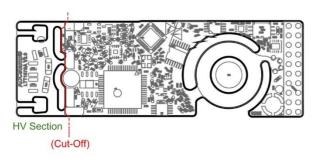


Side View:

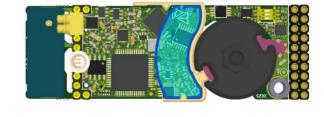




Bottom View:



Bottom View



Primary Connector: Pinout

Description	Name	Pin
IO: max 400kHz, Lo<0.8V, 2V <hi<vdd< td=""><td>I2C_SDA</td><td>1</td></hi<vdd<>	I2C_SDA	1
Connect to protective housing	Chassis	3
OUT: LVDS_P serial shift clk/2 (≤ Vdd)	ADCsclk_P	5
OUT: LVDS_P data ready (≤ Vdd)	ADCdrdy_P	7
OUT: LVDS_P serial data out (≤ Vdd)	ADCdout_P	9
Primary GND level (for Vsup and DigIO)	GNDprim	11
OUT: CMOS digital input @ isolated side	Digital_In	13
IN: LVDS_P SampleClk ≤32MHz (≤ Vdd)	SampleClk_P	15
Primary GND level (for Vsup, Vcc, Vdd)	GNDprim	17
Primary Supply Voltage: 12VDC +/- 5%	12 Vsup	19

Top View	Pin	Name	Description		
	2	I2C_SCL	IN: max 400kHz, Lo<0.8V, 2V <hi<vdd< th=""></hi<vdd<>		
	4 *	Vdd	Primary Digital Supply: 3.1V < Vdd < 3.5V		
	6	ADCsclk_N	OUT: LVDS_N serial shift clk/2 (≤ Vdd)		
	8	ADCdrdy_N	OUT: LVDS_N data ready (≤ Vdd)		
	10	ADCdout_N	OUT: LVDS_N serial data out (≤ Vdd)		
	12	DCDCclk	IN: Lo<0.4V, 0.8V <hi<5.5v, 8<="" sampleclk="" th=""></hi<5.5v,>		
	14	nADCstart	IN: ADCstart of ADS1675 (≤ Vdd)		
	16	SampleClk_N	IN: LVDS_N SampleClk ≤32MHz (≤ Vdd)		
	18	GNDprim	Primary GND level (for Vsup, Vcc, Vdd)		
	20	12 Vsup	Primary Supply Voltage: 12VDC +/- 5%		
300 50 00 / 1 W 00 1 MTINV (110 05 0 D 100)					

Connector 2.54mm grid: 2 x 10 contacts. WPpro 254-020-3-50-00 (mates with Samtec MTLW-110-05-G-D-160)

High Voltage Assembly with HV-Insulation:





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